141663

PRELIMINARY DATA SHEET

INFORMATION STORAGE DEVICES

ISD1200/1400 Series

Single-Chip Voice Record/Playback Devices 10-, 12-, 16-, and 20-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD1200/1400 ChipCorder™ Series provides high-quality, single-chip record/playback solutions to short duration messaging applications. The CMOS devices include an on-chip oscillator, microphone pre-amplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. A minimum record/playback subsystem can be configured with a microphone, a speaker, several passives, two push-buttons, and a power source.

Recordings are stored in nonvolatile memory cells, providing zero-power message storage. This unique solution is made possible through ISD's patented Direct Analog Storage Technology (DAST®), whereby voice and audio signals are stored directly, in their natural analog form, into EEPROM memory. Direct analog storage allows natural voice reproduction in a single-chip solid-state solution.

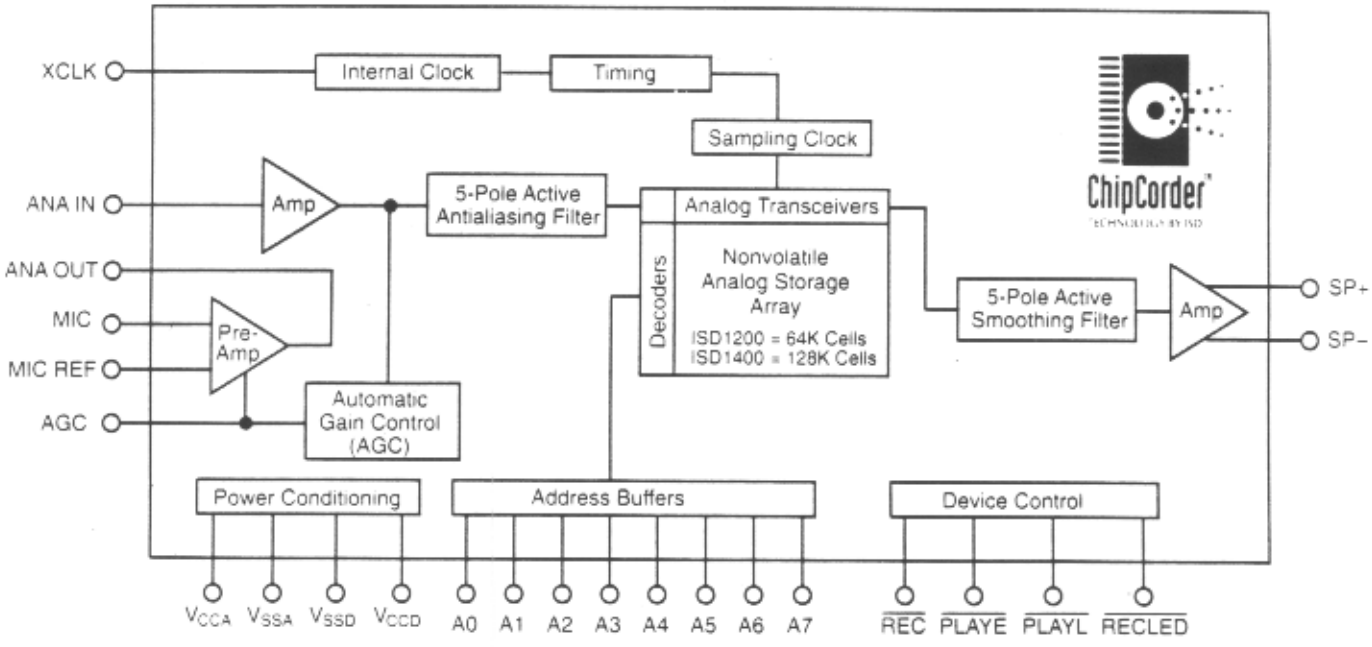
ISD1200/1400 SERIES SUMMARY

Part Number	Minimum Duration (Seconds)	Maximum Input Sample Rate (KHz)	Upper Pass Band (KHz)
ISD1210	10	6.4	2.7
ISD1212	12	5.3	2.3
ISD1416	16	8.0	3.4
ISD1420	20	6.4	2.7

FEATURES

- **Easy-to-use single-chip voice record/playback solution**
  - No external ICs required
  - Minimizes external components
- **High-quality, natural voice/audio reproduction**
- **Push-button interface**
  - Playback can be edge- or level-activated
- **Zero-power message storage**
  - Eliminates battery backup circuits
- **100-year message retention (typical)**
- **100 K record cycles (typical)**
- **On-chip clock source**
- **No programmer or development system needed**
- **Fully addressable to handle multiple messages**
- **Automatic power-down mode**
  - Enters standby mode immediately following a record or playback cycle
  - Standby current 0.5 uA (typical)
- **Single power supply**
- **Available in DIP, SOIC, and die form for Chip-on-Board (COB) Module assembly**

ISD1200/1400 SERIES BLOCK DIAGRAM



DETAILED DESCRIPTION

Basic Operation

The ISD1200/1400 ChipCorder Series devices are controlled by a single signal, $\overline{REC}$, and either of two push-button control playback signals, $\overline{PLAYE}$ (edge-activated playback), and $\overline{PLAYL}$ (level-activated playback). The ISD1200/1400 parts are configured for simplicity of design in a single-message application. Using the address lines will allow multiple message applications. Device operation is explained on page 4.

Speech Quality

ISD's patented DAST technology provides natural record and playback. The input voice signals are stored directly in nonvolatile EEPROM cells, and reproduced without the synthetic effect often heard with digital solid-state speech solutions. A complete sample is stored in a single cell, minimizing the memory necessary to store a recording of a given duration.

Automatic Power-Down Mode

At the end of a playback or record cycle, the ISD1200/1400 Series devices automatically return to a low-power standby mode, consuming typically 0.5 µA. During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after $\overline{REC}$ is released HIGH.

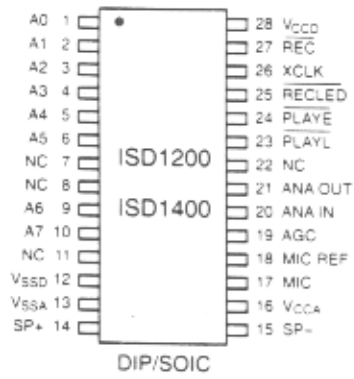
Addressing (optional)

In addition to providing simple message playback, the ISD1200/1400 Series provides a full addressing capability.

The ISD1200 Series storage array has 80 distinct addressable segments, while the ISD1400 Series storage array has 160 distinct addressable segments, providing the following resolutions.

Part Number	Resolution
ISD1210	125 ms
ISD1212	150 ms
ISD1416	100 ms
ISD1420	125 ms

ISD1200/1400 SERIES PINOUTS



Note: NC means Must Not Connect

PIN DESCRIPTIONS

Note: The $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ signals are all debounced for 50 ms. on the rising edge to prevent a false retriggering from a push-button switch.

Record ($\overline{REC}$)

The $\overline{REC}$ input is an active-LOW record signal. The device records whenever $\overline{REC}$ is LOW. This signal must remain LOW for the duration of the recording. $\overline{REC}$ takes precedence over either playback ($\overline{PLAYE}$ or $\overline{PLAYL}$) signal. If $\overline{REC}$ is pulled LOW during a playback cycle, the playback immediately ceases and recording begins.

A record cycle is completed when $\overline{REC}$ is pulled HIGH. An end-of-message marker is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when $\overline{REC}$ goes HIGH.

Playback, Edge-Activated ($\overline{PLAYE}$)

When a LOW-going transition is detected on this input signal, a playback cycle begins. Playback continues until an end-of-message marker is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking $\overline{PLAYE}$ HIGH during a playback cycle will not terminate the current cycle.

Playback, Level-Activated ($\overline{PLAYL}$)

When this input signal transitions from HIGH to LOW, a playback cycle is initiated. Playback continues until $\overline{PLAYL}$ is pulled HIGH, an end-of-message marker is detected, or the end of the device space is reached. The device automatically powers down to standby mode upon completion of the playback cycle.

Note: In playback, if either $\overline{PLAYE}$ or $\overline{PLAYL}$ is held LOW during $\overline{EOM}$ or OVERFLOW, the device will still enter

standby and the internal oscillator and timing generator will stop. However, the rising edge of $\overline{PLAYE}$ and $\overline{PLAYL}$ will no longer be debounced and any subsequent falling edge present on the input pins will initiate another playback.

Record LED Output ($\overline{RECLED}$)

The output $\overline{RECLED}$ is LOW during a record cycle. It can be used to drive an LED to provide feedback that a record cycle is in progress. In addition, $\overline{RECLED}$ pulses LOW momentarily when an end-of-message marker is encountered in a playback cycle.

Microphone Input (MIC)

The microphone is usually AC-coupled to this pin via a series capacitor. The user-selectable value of the input series capacitor (together with the 10K ohm resistance internal to the chip) determines the low-frequency cutoff for the ISD1200/1400 Series passband.

Microphone Reference (MIC REF)

When MIC REF is AC coupled to the microphone ground, the recorded noise level is significantly reduced. Ground noise is referenced to the preamplifier. If this pin is not used, it must NOT be connected to any signal or voltage. It must float.

Analog Output (ANA OUT)

The microphone signal is amplified and is output to the ANA OUT pin. The voltage gain of the preamp is determined by the voltage level at the Automatic Gain Control (AGC) pin. The preamplifier has a maximum gain of about 24 dB for small input signal levels.

Analog Input (ANA IN)

The external capacitor connects ANA IN to the ANA OUT pin. The value of the external capacitor, together with the 3 KΩ input impedance at ANA IN, can be chosen to give additional cutoff at the low-frequency end of the voice passband. The ANA IN pin may also be used to input alternative sources of analog signals (instead of the microphone signal) through a coupling capacitor.

Automatic Gain Control (AGC)

The purpose of the AGC is to dynamically adjust the preamplifier gain, and therefore extend the range of input signals which can be applied to the microphone input without causing distortion. The AGC can considerably extend the range of recordable sound from whispers to loud voices. To use the AGC feature, an external resistor and capacitor should be connected in parallel between the AGC pin and Ground. Recommended values are 470 KΩ and 4.7 µF. The "attack" time of the gain control is determined by the source resistance (5 KΩ) and the external capacitor. The "release" time is determined by the external resistor and capacitor. For AGC voltages of 1.5 Volts and below, the preamplifier is at its maximum gain of 24 dB. Reduction in preamplifier gain occurs for voltages of approximately 1.8 Volts. If the AGC function is not desired, the AGC pin can be tied to Ground and the preamplifier gain will be held at its highest level of approximately 24 dB.

If operating at voltages above 5.5 V, insert a 5.1 KΩ resistor in series with the capacitor from pin 20 to pin 21 to minimize distortion.

Speaker Outputs (SP+, SP–)

The SP+ and SP– pins provide direct drive for loudspeakers with impedances as low as 16 ohms. A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP– are used, a speaker-coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and held at V_{SSA} during Power Down.

Optional External Clock (XCLK)

This signal is normally tied to ground in applications circuits. If, however, greater timing precision is desired, (internal clock has ±2.5 % tolerance over temperature and voltage range), the chip can be externally clocked through this pin. If the XCLK is not used, this input should be connected to ground.

V_{CCA} and V_{CCD}

Analog and digital circuits internal to the ISD1200/1400 Series use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

V_{SSA} and V_{SSD} (Ground)

Similar to V_{CCA} and V_{CCD}, the analog and digital circuits internal to the ISD1200/1400 Series use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

TABLE 1. OPERATIONAL MODES

Address Ctrl. (HIGH)	Function	Typical Use	Jointly* Compatible
A0	Message cueing	Fast-forward through messages	A4
A1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	A3, A4
A2	Unused		
A3	Looping	Continuous playback from Address 0	A1
A4	Consecutive addressing	Record/Play multiple consecutive messages	A0, A1
A5	Unused		

** Indicates additional operational modes which can be used simultaneously with the given mode.*

Address Inputs (A0-A7)

The Address Inputs have two functions, depending upon the level of the two Most Significant Bits (MSB) of the address.

If either of the two MSBs is LOW, the inputs are ALL interpreted as address bits and are used as the start address for the current Record or Playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{PLAYE}$, $\overline{PLAYL}$ or $\overline{REC}$.

OPERATIONAL MODES

The ISD1200/1400 Series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1200/1400 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH, the remaining address signals are interpreted as mode bits and NOT as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1200/1400 address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from Record to Playback, Playback to Record, or when a Power-Down cycle is executed.

Second, an Operational Mode is executed when any of the control inputs, $\overline{PLAYE}$, $\overline{PLAYL}$, or $\overline{REC}$, go LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going control input signal, at which point the current address/mode levels are sampled and executed.

(Note: The two MSBs are on pins 9 and 10 for each ISD1200/1400 Series member.)

OPERATIONAL MODE DESCRIPTIONS

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

A0 — Message Cueing ($\overline{PLAYE}$ or $\overline{PLAYL}$ only)

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each control input LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for Playback only, and is typically used with the A4 Operational Mode.

A1 — Delete $\overline{EOM}$ Markers ($\overline{REC}$ only)

The A1 Operational Mode allows sequentially recorded messages to be concatenated into a single message with only one $\overline{EOM}$ marker set at the end of the combined message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

A2 — Unused

A3 — Message Looping ($\overline{PLAYE}$ or $\overline{PLAYL}$ only)

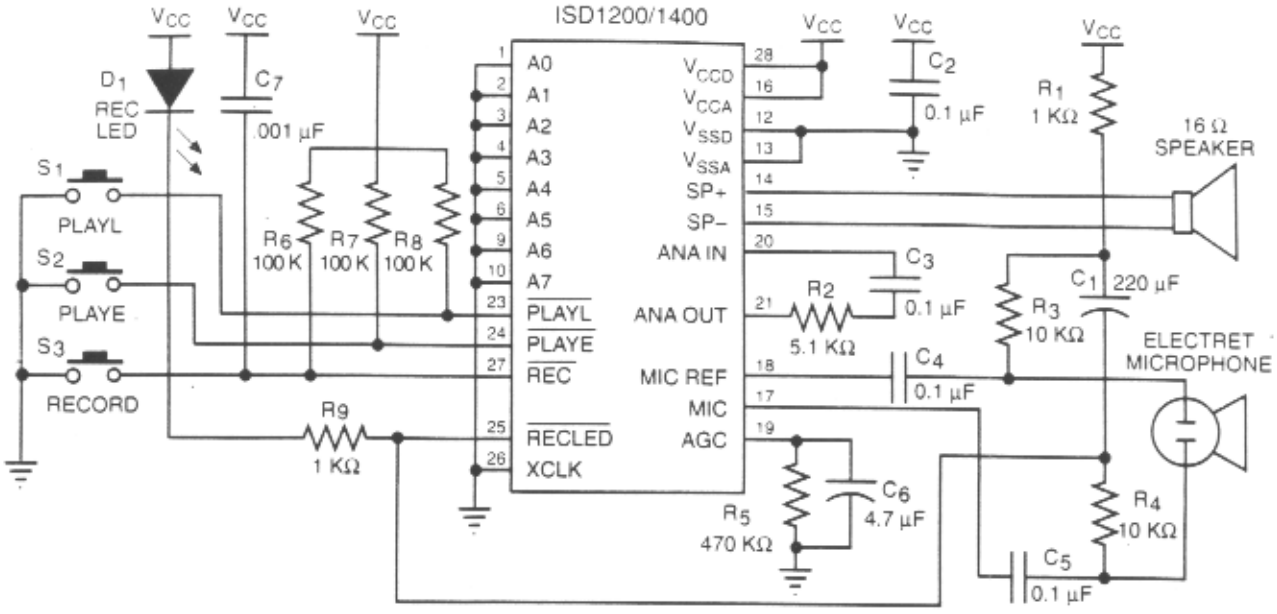
The A3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message CAN completely fill the ISD1200/1400 device and will loop from beginning to end.

A4 — Consecutive Addressing

During normal operations, the address pointer will reset when a message is played through to an $\overline{EOM}$ marker. The A4 Operational Mode inhibits the address pointer reset, allowing messages to be played back consecutively.

A5 — Unused

APPLICATION SCHEMATIC



*Note: **ISD Application Notes and Design Manual** available*

FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1200/1400 Series devices.

1. Record a message filling the address space.

Pulling the $\overline{\text{REC}}$ signal LOW initiates a record cycle from the beginning of the message space. If $\overline{\text{REC}}$ is held LOW, the recording continues until the message space has been filled. Once the message space is filled, recording ceases. The device will automatically power down after $\overline{\text{REC}}$ is pulled HIGH.

2. Edge-activated playback.

Pulling the $\overline{\text{PLAYE}}$ signal LOW initiates a playback cycle from the beginning of the message space. The rising edge of $\overline{\text{PLAYE}}$ has no effect on operation. If a recording has filled the message space, the entire message is played. When the device reaches the end of the message space, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYE}}$ initiates a new play cycle from the start address.

3. Level-activated playback.

Pulling the $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle from the beginning of the message space. If $\overline{\text{PLAYL}}$ remains LOW, the device plays through to the end of the message and subsequently enters the power-down mode.

4. Level-activated playback (truncated).

If $\overline{\text{PLAYL}}$ is pulled HIGH any time during the play-back cycle, the device stops playing and enters the power-down mode. A subsequent falling edge on PLAYL initiates a new play cycle from the start address.

5. Record (interrupting playback).

The $\overline{\text{REC}}$ signal takes precedence over other operations. Any LOW-going transition on $\overline{\text{REC}}$ initiates a new record operation from the beginning of the start address regardless of any current operation in progress.

6. Record a message, partially filling the address space.

A record operation need not fill the entire message space. Releasing the $\overline{\text{REC}}$ signal HIGH before filling the message space causes the recording to stop and an end-of-message marker to be placed. The device powers down automatically.

7. Play back a message, partially filling the address space.

Pulling the $\overline{\text{PLAYE}}$ or $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle which is then completed when the end-of-message marker is encountered. Playback ceases and the device powers down.

8. $\overline{\text{RECLED}}$ operation.

The $\overline{\text{RECLED}}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record in progress" indicator. It returns to a HIGH state when the $\overline{\text{REC}}$ pin is released HIGH or when a recording is completed due to the message space being filled.

APPLICATIONS NOTE

Some users may experience an unexpected recording taking place when their circuit is powered up, or the batteries are changed and V_{CC} rises faster than REC. This undesired recording prevents playback of the previously recorded message. A spurious End Of Message ($\overline{EOM}$) marker appears at the very beginning of the memory, preventing access to the original message, and nothing is played.

To prevent this occurrence, place a capacitor (approx. .001 µF) between the control pin ($\overline{REC}$) and V_{CC}. This pulls the control pin voltage up with V_{CC} as it rises. Once the voltage is HIGH, the pull-up device will keep the pin HIGH until intentionally pulled LOW, preventing the false $\overline{EOM}$ marker.

Since this anomaly is dependent upon factors such as the capacitance of the user's printed circuit board, not all circuit designs will exhibit the spurious marker. It is recommended, however, that the capacitor is included for design reliability. A more detailed explanation and resolution of this occurrence is described in the **ISD Application Notes and Design Manual.**

ABSOLUTE MAXIMUM RATINGS (ISD1200/1400 SERIES – PACKAGED)

Condition	Value
Temperature under bias	- 65° C to + 125° C
Storage temperature range	- 65° C to + 150° C
Voltage applied to any pin	(V_{SS} - 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ± 20 mA)	(V_{SS} - 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering - 10 seconds)	300° C
V_{CC} - V_{SS}	- 0.3 V to + 7.0 V

Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability.

DC PARAMETERS (ISD1200/1400 SERIES – PACKAGED)

Operating Conditions: T_A = 0° to 70° C, V_{CC} = 4.5 V to 6.5 V (1), V_{SS} = 0 V (2); unless otherwise noted

Symbol	Parameters	Min	Typ (3)	Max	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = - 1.6 mA
I_{CC}	V_{CC} Current @ 5.5 V (Operating)		15	30	mA	V_{CC} = 5.5 V, R_{EXT} = ∞ (4)
I_{CC}	V_{CC} Current @ 6.5 V (Operating)		15	35	mA	V_{CC} = 6.5 V, R_{EXT} = ∞ (4)
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	(4) (5)
I_{IL}	Input Leakage Current			±1	µA	(4) (5)
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} (6) (7)
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
R_{ANA} In	Ana In Input Resistance		3		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		- 45	- 15	dB	AGC = 2.5 V
A_{ARP}	Ana In to SP+/-		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Preamp Out Source		- 2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

Notes: 1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.
3. Typical values @ T_A = 25° C and 5.0 V.
4. V_{CCA} and V_{CCD} connected together.
5. $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be V_{CCD}.
6. Pin 26.
7. Applies only to ISD1200 and ISD1400 future version (see page 13).

AC PARAMETERS (ISD1200/1400 SERIES – PACKAGED)

Operating Conditions: T_A = 0° to 70° C, V_{CC} = 4.5 V to 6.5 V [1], V_{SS} = 0 V [2]; unless otherwise noted

Symbol	Characteristic	Min	Typ [3]	Max	Units	Conditions
THD	Total Harmonic Distortion		1		%	@ 1 KHz
T_{LED1}	$\overline{\text{RECLED}}$ ON Delay		5		µsec	
T_{LED2}	$\overline{\text{RECLED}}$ OFF Delay		48.6		msec	
T_S	A3 Loop Setup Time	300			nsec	
T_H	A3 Loop Hold Time	0			nsec	
T_{RPUD}	Record Power-Up Delay		32		msec	
T_{RPDD}	Record Power-Down Delay		32		msec	
T_{PPUD}	Play Power-Up Delay		32		msec	
T_{PPDD}	Play Power-Down Delay		8.1		msec	
P_{OUT}	Speaker Output Power		12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins		1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage			20	mV	Peak-to-Peak [4]
V_{IN2}	ANA IN Input Voltage			50	mV	Peak-to-Peak

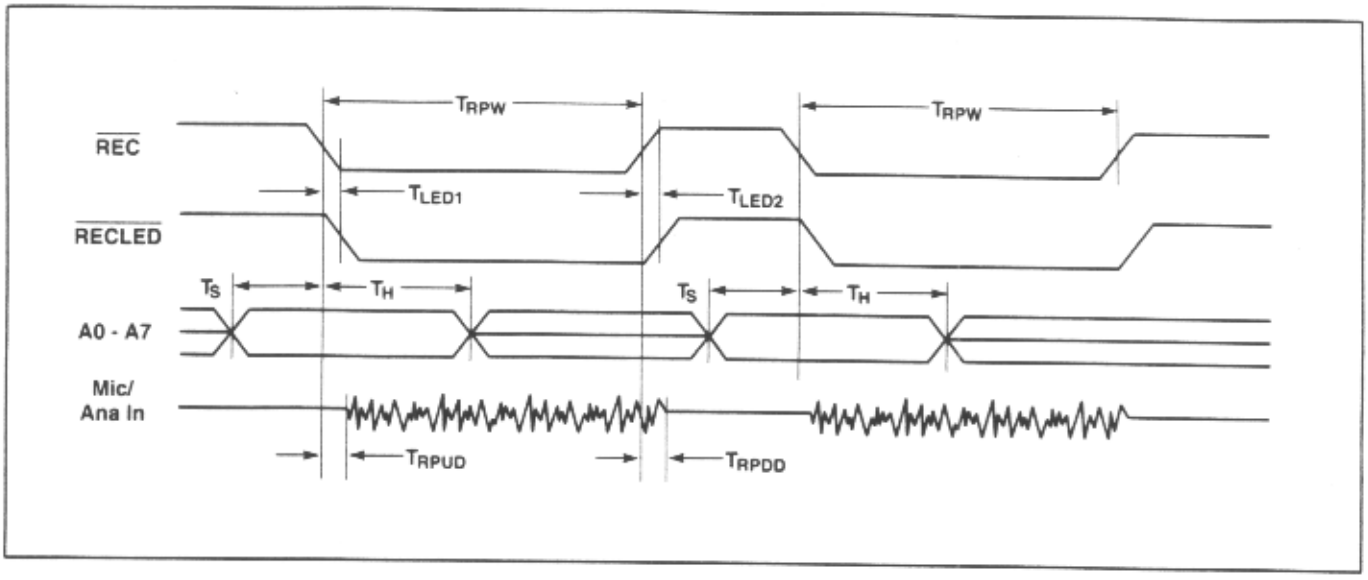
AC PARAMETERS

Symbol	Characteristic	ISD-1210	ISD-1212	ISD-1416	ISD-1420	Units	Conditions
F_S	Sampling Frequency (max)	6.4	5.3	8	6.4	KHz	Internal Oscillator
BW	Bandwidth (max)	2.7	2.3	3.4	2.7	KHz	3 dB Roll-Off Point [5]
T_{RPW}	Record Pulse Width (max)	10	12	16	20	sec.	
T_{PLAY}	Playback Duration (min)	10	12	16	20	sec.	
T_{LED2}	$\overline{\text{RECLED}}$ OFF Delay	48.6	58.3	38.9	48.6	msec	[6]
T_{RPUD}	Rec. Power-Up Delay	32	39	26	32	msec	[6]
T_{RPDD}	Rec. Power-Down Delay	32	39	26	32	msec	[6]
T_{PPUD}	Play Power-Up Delay	32	39	26	32	msec	[6]
T_{PPDD}	Play Power-Down Delay	8.1	9.7	6.5	8.1	msec	[6]

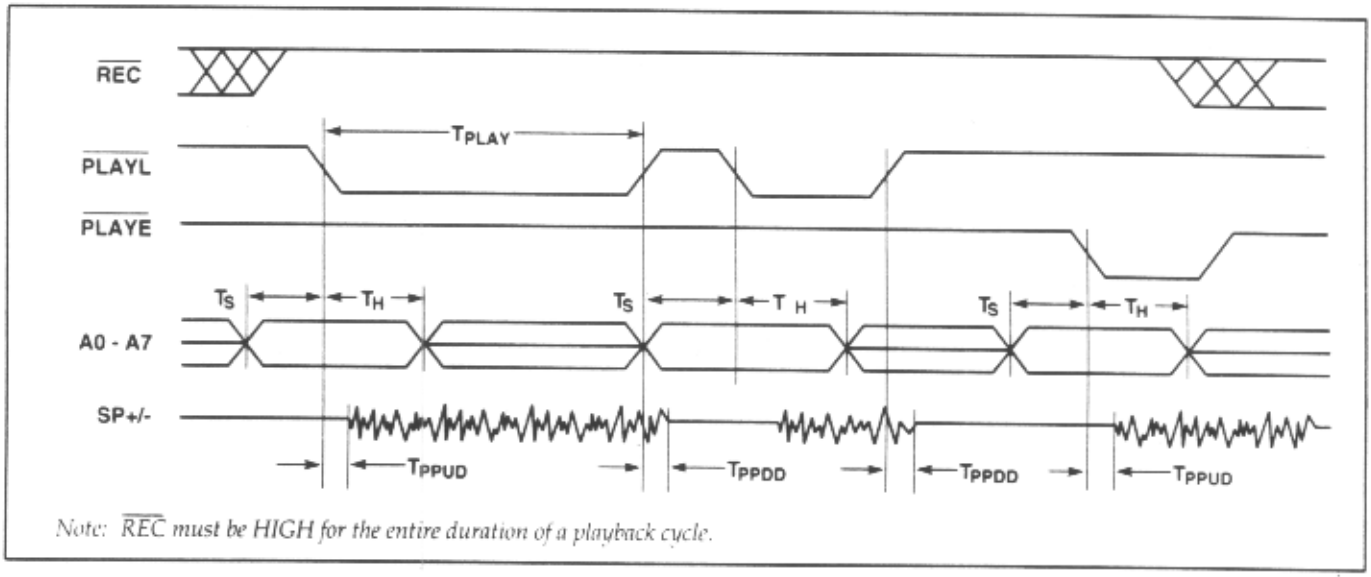
Notes: 1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.
3. Typical values @ T_A = 25° C, 5.0 V, and 6.2 KHz sample rate.
4. With 12 KΩ series resistor at ANA IN.
5. Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).
6. Typical values @ T_A = 25° C and 5.0 V.

TIMING DIAGRAMS (ISD1200/1400 SERIES – PACKAGED)

RECORD



PLAYBACK



Note: $\overline{REC}$ must be HIGH for the entire duration of a playback cycle.

ABSOLUTE MAXIMUM RATINGS (ISD1200X/1400X SERIES - UNPACKAGED DIE)

Condition	Value
Storage temperature range	- 65°C to 150°C
Voltage applied to any pin	(V_{SS} - 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ± 20 mA)	(V_{SS} - 1.0 V) to (V_{CC} + 1.0 V)
V_{CC} - V_{SS}	- 0.3 V to + 7.0 V

Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability.

DC PARAMETERS (ISD1200X/1400X SERIES - UNPACKAGED DIE)

Operating Conditions: T_A = 0° to 50° C (ambient), V_{CC} = 4.5 V to 6.5 V (1), V_{SS} = 0 V (2); unless otherwise noted

Symbol	Parameters	Min	Typ (3)	Max	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = - 1.6 mA
I_{CC}	V_{CC} Current @ 5.5 V (Operating)		15	30	mA	V_{CC} = 5.5 V, R_{EXT} = ∞ (4)
I_{CC}	V_{CC} Current @ 6.5 V (Operating)		15	35	mA	V_{CC} = 6.5 V, R_{EXT} = ∞ (4)
I_{SB}	V_{CC} Current (Standby)		0.5	10	µA	(4) (5)
I_{IL}	Input Leakage Current			±1	µA	(4) (5)
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} (6) (7)
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
R_{ANA} In	Ana In Input Resistance		3		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		- 45	- 15	dB	AGC = 2.5 V
A_{ARP}	Ana In to SP+/-		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Preamp Out Source		- 2		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.5		mA	@ V_{OUT} = 2.0 V

Notes: 1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.
3. Typical values @ T_A = 25° C and 5.0 V.
4. V_{CCA} and V_{CCD} connected together.
5. $\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be V_{CCD}.
6. Pin 26.
7. Applies only to ISD1200 and ISD1400 future version (see page 13).

AC PARAMETERS (ISD1200X/1400X SERIES – UNPACKAGED DIE)

Operating Conditions: T_A = 0° to 50° C (ambient), V_{CC} = 4.5 V to 6.5 V [1], V_{SS} = 0 V [2]; unless otherwise noted

Symbol	Characteristic	Min	Typ [3]	Max	Units	Conditions
THD	Total Harmonic Distortion		1		%	@ 1 KHz
t_{LED1}	$\overline{\text{RECLED}}$ ON Delay		5		µsec	
t_{LED2}	$\overline{\text{RECLED}}$ OFF Delay		48.6		msec	
t_{AS}	A3 Loop Setup Time	300			nsec	
t_{AH}	A3 Loop Hold Time	0			nsec	
t_{RPUD}	Record Power-Up Delay		32		msec	
t_{RPDD}	Record Power-Down Delay		32		msec	
t_{PPUD}	Play Power-Up Delay		32		msec	
t_{PPDD}	Play Power-Down Delay		8.1		msec	
P_{OUT}	Speaker Output Power		12.2		mW	R_{EXT} = 16 Ω
V_{OUT}	Voltage Across Speaker Pins		1.25	2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	MIC Input Voltage			20	mV	Peak-to-Peak [4]
V_{IN2}	ANA IN Input Voltage			50	mV	Peak-to-Peak

AC PARAMETERS

Symbol	Characteristic	ISD-1210	ISD-1212	ISD-1416	ISD-1420	Units	Conditions
F_S	Sampling Frequency (max)	6.4	5.3	8	6.4	KHz	Internal Oscillator
BW	Bandwidth (max)	2.7	2.3	3.4	2.7	KHz	3 dB Roll-Off Point [5]
T_{RPW}	Record Pulse Width (max)	10	12	16	20	sec.	
T_{PLAY}	Playback Duration (min)	10	12	16	20	sec.	
T_{LED2}	$\overline{\text{RECLED}}$ OFF Delay	48.6	58.3	38.9	48.6	msec	[6]
T_{RPUD}	Rec. Power-Up Delay	32	39	26	32	msec	[6]
T_{RPDD}	Rec. Power-Down Delay	32	39	26	32	msec	[6]
T_{PPUD}	Play Power-Up Delay	32	39	26	32	msec	[6]
T_{PPDD}	Play Power-Down Delay	8.1	9.7	6.5	8.1	msec	[6]

Notes: 1. $V_{CC} = V_{CCA} = V_{CCD}$.
2. $V_{SS} = V_{SSA} = V_{SSD}$.
3. Typical values @ T_A = 25° C, 5.0 V, and 6.2 KHz sample rate.
4. With 12 KΩ series resistor at ANA IN.
5. Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).
6. Typical values @ T_A = 25° C and 5.0 V.

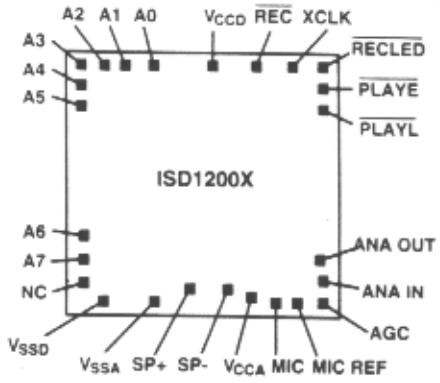
ISD1200X DIE BONDING PHYSICAL LAYOUT

ISD1200X

I. Die Dimensions
X: 172.2 ±1 mils
Y: 138.2 ±1 mils

II. Die Thickness
21 mils

III. Pad Opening (min)
88 x 112 microns
(3.46 x 4.41 mils)



ISD1200X PIN/PAD DESIGNATIONS, WITH RESPECT TO DIE CENTER (μm)

Pin	Pin Name	X Axis	Y Axis	Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1364	1589.6	V_{CCA}	V_{CC} Analog Power Supply	780	-1552.4
A1	Address 1	-1648.4	1589.6	MIC	Microphone Input	992	-1590
A2	Address 2	-1816.4	1589.6	MIC REF	Microphone Reference	1169.2	-1590
A3	Address 3	-2013.6	1515.6	AGC	Automatic Gain Control	1978.4	-1590
A4	Address 4	-2013.6	1337.6	ANA IN	Analog Input	2005.6	-1196.4
A5	Address 5	-2013.6	1129.6	ANA OUT	Analog Output	1991.2	-995.2
A6	Address 6	-2013.6	-831.2	$\overline{PLAYL}$	Level-Activated Playback	2014.4	1224.4
A7	Address 7	-2013.6	-1022	$\overline{PLAYE}$	Edge-Activated Playback	2014.4	1392.8
NC	No Connect	-2013.6	-1361.6	$\overline{RECLED}$	Record LED Output	2012.4	1587.6
V_{SSD}	V_{SS} Digital Power Supply	-1893.6	-1588	XCLK	No Connect (optional)	1581.2	1589.6
V_{SSA}	V_{SS} Analog Power Supply	-357.6	-1588	$\overline{REC}$	Record	752.8	1589.6
SP+	Speaker Output +	-17.2	-1512.8	V_{CCD}	V_{CC} Digital Power Supply	-48	1545.2
SP–	Speaker Output –	412.4	-1512.8				

Note: Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.

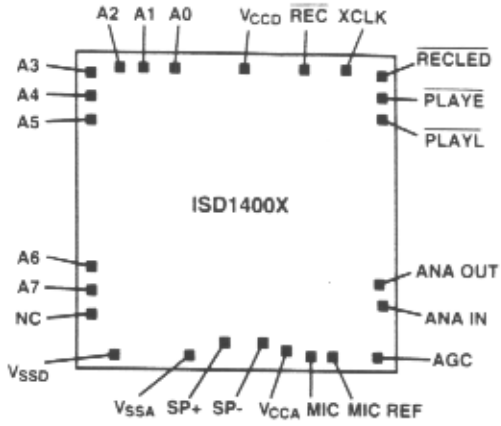
ISD1400X CURRENT DIE BONDING PHYSICAL LAYOUT

ISD1400X

I. Die Dimensions
X: 211 ±1 mils
Y: 207 ±1 mils

II. Die Thickness
21 mils

III. Pad Opening (min)
109 microns
(4.3 mils)



ISD1400X PIN/PAD DESIGNATIONS, WITH RESPECT TO DIE CENTER (μm)

Pin	Pin Name	X Axis	Y Axis	Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1712.5	2445.5	V_{CCA}	V_{CC} Analog Power Supply	952.2	-2412
A1	Address 1	-2068	2445.5	MIC	Microphone Input	1217.5	-2459
A2	Address 2	-2278	2445.5	MIC REF	Microphone Reference	1439	-2459
A3	Address 3	-2509.5	2368	AGC	Automatic Gain Control	2450.5	-2410
A4	Address 4	-2509.5	2145.5	ANA IN	Analog Input	2484.5	-1980.5
A5	Address 5	-2509.5	1885.5	ANA OUT	Analog Output	2466.5	-1715.5
A6	Address 6	-2509.5	-1525.5	$\overline{\text{PLAYL}}$	Level-Activated Playback	2495.5	1989
A7	Address 7	-2509.5	-1764	$\overline{\text{PLAYE}}$	Edge-Activated Playback	2495.5	2201
NC	No Connect	-2509.5	-2178.5	$\overline{\text{RECLED}}$	Record LED Output	2493	2443
V_{SSD}	V_{SS} Digital Power Supply	-2359.5	-2456.5	XCLK	No Connect (optional)	1970	2445.5
V_{SSA}	V_{SS} Analog Power Supply	-469.5	-2456.5	$\overline{\text{REC}}$	Record	900	2445.5
SP+	Speaker Output +	-29	-2362.5	V_{CCD}	V_{CC} Digital Power Supply	-52.5	2390
SP–	Speaker Output –	508	-2362.5				

Note: Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.

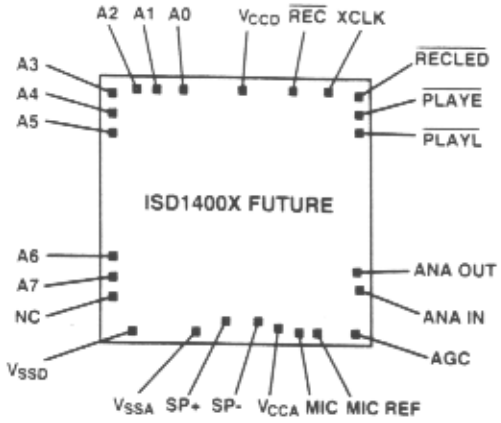
ISD1400X FUTURE DIE BONDING PHYSICAL LAYOUT

ISD1400X FUTURE

I. Die Dimensions
X: 206.9 +1 mils
Y: 202.3 +1 mils

II. Die Thickness
21 mils

III. Pad Opening (min)
100 x 112 microns
(3.9 x 4.4 mils)



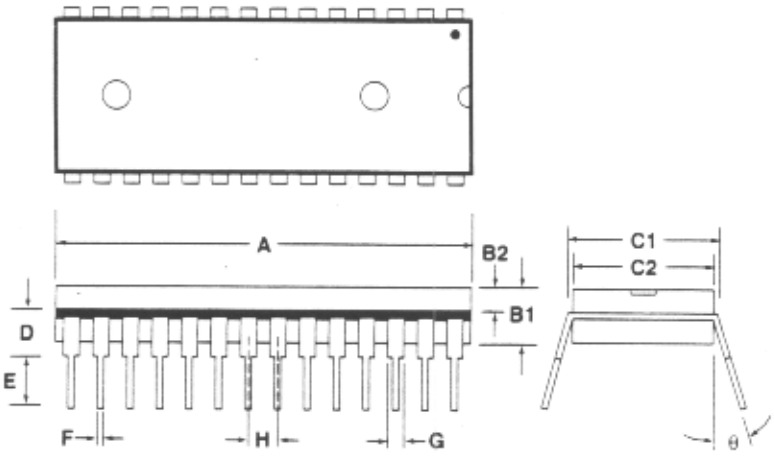
ISD1400X FUTURE PIN/PAD DESIGNATIONS, WITH RESPECT TO DIE CENTER (μm)

Pin	Pin Name	X Axis	Y Axis	Pin	Pin Name	X Axis	Y Axis
A0	Address 0	-1332.5	1973.8	V_{CCA}	V_{CC} Analog Power Supply	779.5	-1936.2
A1	Address 1	-1628.9	1973.8	MIC	Microphone Input	991.5	-1973.8
A2	Address 2	-1808.9	1973.8	MIC REF	Microphone Reference	1168.7	-1973.8
A3	Address 3	-2014.1	1910.2	AGC	Automatic Gain Control	1977.9	-1910.6
A4	Address 4	-2014.1	1722.6	ANA IN	Analog Input	2005.1	-1580.2
A5	Address 5	-2014.1	1519.8	ANA OUT	Analog Output	1990.7	-1379
A6	Address 6	-2014.1	-1214.6	$\overline{PLAYL}$	Level-Activated Playback	2013.9	1608.6
A7	Address 7	-2014.1	-1399.8	$\overline{PLAYE}$	Edge-Activated Playback	2013.9	1777
NC	No Connect	-2014.1	-1745.4	$\overline{RECLED}$	Record LED Output	2011.9	1971.8
V_{SSD}	V_{SS} Digital Power Supply	-1894.1	-1971.8	XCLK	No Connect (optional)	1580.7	1973.8
V_{SSA}	V_{SS} Analog Power Supply	-358.1	-1971.8	$\overline{REC}$	Record	752.3	1973.8
SP+	Speaker Output +	-17.7	-1896.6	V_{CCD}	V_{CC} Digital Power Supply	-48.5	1929.4
SP–	Speaker Output –	411.9	-1896.6				

Note: Die dimensions and pin/pad positions may be subject to change. Please contact ISD Sales Offices or Representatives to verify current or future specifications.

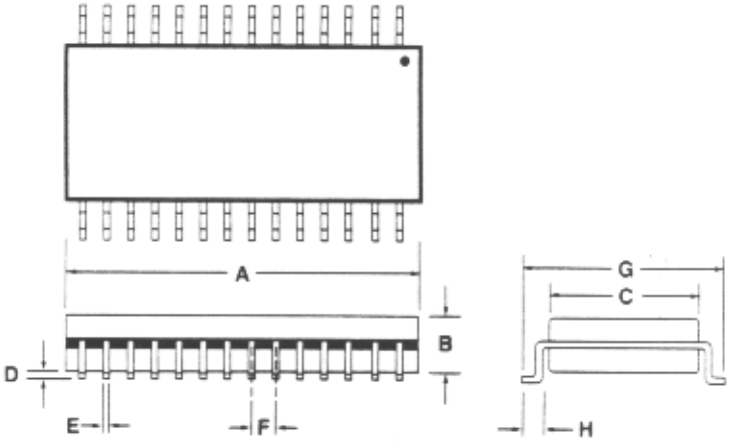
PACKAGE DIAGRAMS

28-Lead Plastic Dual In-Line Package (DIP) Type P



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.7	36.83	36.95
B1		.150			3.81	
B2	.065	.070	.075	1.65	1.78	1.91
C1	.600		.625	15.24		15.88
C2	.530	.540	.550	13.46	13.72	13.97
D	.115	.120	.125	2.92	3.05	3.18
E	.125	.130	.135	3.18		3.43
F	.015	.018	.022	0.38	0.46	0.56
G	.055	.060	.065	1.40	1.52	1.65
H		.100			2.54	
θ	0°	7°	15°	0°	7°	15°

28-Lead Plastic Small Outline Package (SOIC) Type J



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	.706	.714	.718	17.93	18.14	18.24
B	.086	.088	.090	2.18	2.24	2.29
C	.340	.346	.350	8.64	8.79	8.89
D	.004	.007	.010	.102	.178	.254
E	.014	.016	.020	.360	.410	.480
F		.050			1.27	
G	.463	.470	.477	11.76	12.00	12.12
H	.020	.031	.042	.510	.790	1.07

ORDERING INFORMATION

When placing an order for the ISD1200/1400 Series devices, please refer to the following part numbers:

Part No.	Rec/Play Duration	Description
ISD1210P	10 sec.	28-pin plastic dual in-line package (DIP)
ISD1210G	10 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1210X	10 sec.	Bare unpackaged die
ISD1212P	12 sec.	28-pin plastic dual in-line package (DIP)
ISD1212G	12 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1212X	12 sec.	Bare unpackaged die
ISD1416P	16 sec.	28-pin plastic dual in-line package (DIP)
ISD1416G	16 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1416X	16 sec.	Bare unpackaged die
ISD1420P	20 sec.	28-pin plastic dual in-line package (DIP)
ISD1420G	20 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1420X	20 sec.	Bare unpackaged die

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